Cache Project Feedback

read\_miss state design is not right.

When read\_miss, you'll need to updata cache.

Before updating cache, you need to check

dirty bit and valid bit of the cache. If both are logic 1s,

you'll need to write the cache data into main memory.

And then read data from the Main memory.

While reading from main memory,

you can think about the Main memory as target

and Cache controler as master.

So master sends out MStrobe to inform main memory to start transaction,

and also use MRW to indicate read operation.

It needs to check MReady until it is ready (target ready) to complete

reading out data from Main memory. Then it can pass data to CPU and

also update Cache.

Minimum deduction: 5 points.

Similaly in write\_miss state,

the cache controller needs to first sends out MStrobe to inform main memory to start transaction,

and also use MRW to indicate write operation when dirty bit is 1.

It needs to check MReady until it is ready (target ready) which means writing main memory

is done.

Then it can update Cache.

Minimum deduction: 5 points.

Your project 2 grade: 90